What is claimed is:

1. A variable threshold voltage complementary MOSFET with a SOI structure comprising:

a SOI substrate main body having a support substrate, an insulating layer disposed on the support substrate, and island-shaped first and second silicon layers separately formed on the insulating layer;

a first MOSFET formed of a fully depleted SOI where a first channel part is formed in the first silicon layer;

a second MOSFET formed of a partially depleted SOI where a second channel part is formed in the second silicon layer, the second MOSFET configuring a complementary MOSFET with the first MOSFET; and

an adjusted bias electrode disposed on the support substrate for applying an adjusted bias voltage to adjust threshold voltage of the complementary MOSFET to the SOI substrate main body.

2. The variable threshold voltage complementary MOSFET with the SOI structure according to claim 1,

wherein the first MOSFET has a first source region and a first drain region formed in the first silicon layer as they sandwich the first channel part, and a first gate electrode disposed on the first channel part as they sandwich a first gate insulating film; and

the second MOSFET has a second source region and a second

drain region in the second silicon layer as they sandwich the second channel part, a second gate electrode formed on the second channel part as they sandwich a second gate insulating film, a region in the second silicon layer where a depletion layer is not formed, the region is a neutral region for suppressing adjusting threshold voltage of the second MOSFET by the adjusted bias voltage, and a suppressed voltage electrode disposed so as to contact with the neutral region for applying suppressed voltage to suppress the threshold voltage to the neutral region.

3. The variable threshold voltage complementary MOSFET with the SOI structure according to claim 1 or 2, wherein the first MOSFET is an N-channel MOSFET and the second MOSFET is a P-channel MOSFET.

4. The variable threshold voltage complementary MOSFET with the SOI structure according to claim 1 or 2, wherein the first MOSFET is a P-channel MOSFET and the second MOSFET is an N-channel MOSFET.